

This listing of claims will replace all prior versions and listings of claims in the application.

### **LISTING OF CLAIMS**

What is claimed is:

1. (Currently amended) A semiconductor ~~device~~package, comprising:  
  
at least one semiconductor chip ~~having at least one~~ comprising a lateral power transistor device formed therein~~[[;]], said semiconductor chip having an upper surface and a one or more source, and drain terminal~~~~[[s]] disposed on said upper surface thereof, each of said source and drain terminal~~~~[[s]] having a conductive bump selected from the group consisting of a ball bump~~~~[[or]] and a pillar bump disposed thereon;~~  
  
a metal lead frame spanning said upper surface of said semiconductor chip, said metal lead frame being in electrical contact with said conductive ~~balls or pillar bump~~~~[[s]]~~; and  
  
a capsule encasing said semiconductor chip and at least a portion of said metal lead frame.
2. (Currently amended) The semiconductor package as in claim 1 wherein ~~said chip further comprises a one or more~~ the terminal is selected from the group consisting of a source terminal, a drain terminal, and a gate terminals on said upper surface thereof; ~~each of said gate terminals having a conductive ball or pillar bump thereon.~~
3. (Currently amended) The semiconductor package as in claim 1 wherein ~~[[said]]~~ opposite ends of said metal lead frame protrude~~[[s]]~~ from opposite sides of said capsule.

4. (Currently amended) The semiconductor package as in claim 1 wherein said pillar bump[[s]] comprises copper and a conductive solder.
5. (Currently amended) The semiconductor package as in claim 1 wherein said conductive ball[[s]] comprises a conductive solder.
6. (Original) The semiconductor package as in claim 1 wherein said lateral power transistor device comprises a lateral power metal oxide field effect transistor.
7. (Original) The semiconductor package as in claim 1 wherein said lead frame comprises a conductive metal.
8. (Currently amended) The semiconductor package as in claim [[2]]7 wherein said conductive metal comprises copper.
9. (Original) The semiconductor package as in claim 1 wherein said capsule comprises a non-conductive molding compound.
10. (Currently amended) The semiconductor package as in claim [[9]]1 wherein said capsule comprises a plastic.
11. (Currently amended) The semiconductor package as in claim[[s 3]]1 wherein said electrical contact is formed by conductive solder compris[[es]]ing at least one of tin and epoxy.
12. (Currently amended) A semiconductor ~~device~~package, comprising:  
  
at least one monolithic semiconductor structure having at least one comprising a pair of lateral power transistor devices formed ~~combined~~ on a single semiconductor substrate ~~formed therein~~; said semiconductor structure having an

upper surface and ~~a one or more source and drain terminal~~[[s]] disposed on said upper surface thereof; ~~each of said source and drain terminal~~[[s]] having a conductive bump selected from the group consisting of a ball bump [[or]] and a pillar bump disposed thereon;

a metal lead frame spanning said upper surface of said [[chip]]semiconductor structure, said metal lead frame being in electrical contact with said conductive ~~balls or pillar bump~~[[s]]; and

a capsule encasing said [[chip]]semiconductor structure and at least a portion of said metal lead frame.

13. (Currently amended) The semiconductor package as in claim 12 wherein ~~said structure further comprises one or more~~ the terminal is selected from the group consisting of a source terminal, a drain terminal, and a gate terminals on said upper surface thereof; each of said gate terminals having a conductive ball or pillar bump thereon.
14. (Currently amended) The semiconductor package as in claim 12 wherein [[said]] opposite ends of said metal lead frame protrude[[s]] from opposite sides of said capsule.
15. (Currently amended) The semiconductor package as in claim 12 wherein said pillar bump[[s]] comprise copper and a conductive solder.
16. (Currently amended) The semiconductor package as in claim 12 wherein said conductive ball[[s]] comprises a conductive solder.
17. (Original) The semiconductor package as in claim 12 wherein said lateral power transistor device comprises a lateral power metal oxide field effect transistor.

18. (Original) The semiconductor package as in claim 12 wherein said lead frame comprises a conductive metal.
19. (Original) The semiconductor package as in claim 18 wherein said conductive metal comprises copper.
20. (Original) The semiconductor package as in claim 12 wherein said capsule comprises a non-conductive molding compound.
21. (Currently amended) The semiconductor package as in claim ~~[[20]]~~12 wherein said capsule comprises plastic.
22. (Currently amended) The semiconductor package as in claim 12 wherein said lateral power transistor device comprises ~~one or more~~ an analog integrated circuit.
23. (Original) The semiconductor package as in claim 12 wherein said lateral power transistor device comprises an integrated MOSFET and analog circuit structure.
24. (Currently amended) The semiconductor package as in claim 1 wherein said lateral power transistor device comprises ~~one or more~~ an analog integrated circuit~~[[s]]~~.
25. (Original) The semiconductor package as in claim 1 wherein said lateral power transistor device comprises an integrated MOSFET and analog circuit structure.
26. (New) The semiconductor package as in claim 1, wherein the semiconductor package comprises a plurality of the semiconductor chips.
27. (New) The semiconductor package as in claim 1, wherein the semiconductor chip comprises a plurality of the lateral power transistor devices formed therein.

28. (New) The semiconductor package as in claim 1, wherein the lateral power transistor comprises a plurality of terminals disposed on said upper surface, the plurality of terminals comprising a source terminal, a drain terminal, and a gate terminal, each of said source, drain, and gate terminals having a conductive bump selected from the group consisting of a ball bump and a pillar bump disposed thereon.
29. (New) The semiconductor package as in claim 12, wherein the semiconductor package comprises a plurality of the monolithic semiconductor structures.
30. (New) The semiconductor package as in claim 12, wherein the monolithic semiconductor structure comprises a plurality of the pairs of lateral power transistor devices formed on a single semiconductor substrate.
31. (New) The semiconductor package as in claim 12, wherein each of the lateral power transistor devices comprises a plurality of terminals disposed on said upper surface, the plurality of terminals comprising a source terminal, a drain terminal, and a gate terminal, each of said source, drain, and gate terminals having a conductive bump selected from the group consisting of a ball bump and a pillar bump disposed thereon.